**Bachelor Thesis:**

**Design and Verification of the Transport Layer for a Standardized High Speed Serial Interface (JESD204B) using SystemVerilog**

Modern biomedical smart-sensor ICs follow a general trend in microelectronic. They create more and more data (e.g. next-generation “NeuroChip” will produce several Gb/s), which in consequence makes “On-Chip” analog-digital conversion mandatory. The JESD204A/B industry standard was developed recently (2011) by the JEDEC association to address the problem of interconnecting wideband or high data-rate converters with other system chips (e.g. FPGAs) in an efficient and cost saving manner. The transport layer (layer 4 in the OSI-model) maps the conversion samples of multiple A/D-converters of the same IC in a data frame which will be transmitted to the next layer (link layer).

SystemVerilog is an official IEEE standard (most recent version is IEEE 1800-2017) and has been called the industry’s first Hardware Description and Verification Language (HDVL), because it combines the features of Hardware Description Languages such as Verilog and VHDL with features from specialised Hardware Verification Languages, together with features from C and C++.

This work offers the chance to gain insight in the development flow for digital circuits. Both aspects (design and verification) can be studied by using the most recent design methods and techniques (e.g. assertion-based verification, SVA, UVM).

**Supervisor:** Norman Dodel  
**Contact:** norman.dodel@tu-berlin.de  
**Start:** Immediately  
**E 214 📞 28671**

---

Berlin, February 26, 2018