CCO-Based Continuous-Time ΔΣ Modulators for Electrochemical Sensor Arrays

System- and transistor-level simulation results

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***Abstract*—A 1st order current-mode continuous-time delta-sigma modulator architecture is presented for in-sensor-site readout in electrochemical sensor arrays. The electrode-to-electrolyte interface is used as integration capacitance, followed by a Current-Controlled Oscillator-based quantizer. A relaxation oscillator is optimized to meet the requirements of Cyclic Voltammetry. Two circuit realizations are presented and investigated by means of simulation. Both modulators achieve 30 dB/decade noise shaping and reach an SNDR of 67 dB and 62 dB, respectively, at a signal bandwidth of 10 kHz. The reported modulators are highly efficient regarding area and power, and immune to noise and supply voltage variations.**

***Keywords*—Delta Sigma modulator; CCO-based quantizer; electrochemical detection; relaxation oscillator; Cyclic Voltammetry.**

I. INTRODUCTION

Sensor arrays with in-sensor-site A/D conversion are used in imaging, biochemical sensing, and further application areas [1-6]. Many of them, especially CMOS-based microarrays for electrochemical bio molecule detection [1, 2], operate under the boundary conditions of low frequency input signals, current-domain signal representation, and limited available area per sensor site.

Electrochemical detection requires the use of potentiostatic readout circuitry and of a working electrode – which is the interface to the electrolyte – in every sensor site. The readout circuit controls the electrode voltage and measures a low frequency input current from this electrode. The low frequency input signal suggests the Delta-Sigma (ΔΣ) conversion principle, since high oversampling ratios can be reached at moderate clock frequencies. This means that high resolution can be reached while the power consumption is kept low, in particular if a continuous time ΔΣ converter is used. Moreover, area requirements are relatively low as well thanks to the moderate demands of ΔΣ ADCs concerning their analog circuit parts.

Current-controlled oscillator based A/D conversion is highly area- and power-efficient and offers advantages like high immunity to external noise [7] and low supply voltage operation capability [8]. Both properties make Current-Controlled Oscillators (CCOs) suitable to be integrated within arrays with relatively small sensor site pitches, where the supply voltage may vary from site to site and decrease towards the center of the array.

The sensor interface circuitry has to fulfill further requirements related to the specific readout technique: for instance, glitches of the electrode voltage have to be avoided or at least their amplitude has to be kept below a certain minimum. Electrode voltage ripples may result from using an oscillator to quantize the electrode signal and must be kept sufficiently low as well. Due to device parameter variations and further imperfections, an offset may exist between the actual electrode voltage and the desired one. This offset may also vary statistically from site to site within the sensor array. Also such non-idealities must not exceed certain limits and have to be taken into account by robust design and layout .

In this work, we present a current-mode continuous time current-controlled oscillator (CCO)-based ΔΣ modulator which is adapted to the requirements of readout circuits in electrochemical sensor arrays. The proposed topology is designed on system- and on transistor-level and verified by simulation. Two approaches are investigated: the first one using a well-known relaxation oscillator structure, and the second one using a modified relaxation oscillator to respond to the specific requirements of a specific electrochemical detection principle, Cyclic Voltammetry [9]. This principle requires a readout circuit which is able to sweep the electrode voltage over a range of approximately 500 mV.

In the following, the related modulators are considered under the condition of 10 kHz bandwidth at 6 MHz sampling frequency, which are typical values for the aspired application.

II. READOUT CIRCUIT TOPOLOGY AND BLOCK DESIGN

The architecture of a 1st order oscillator-based ΔΣ-modulator is depicted in Fig. 1 [10]. The analog integrator represents the first stage which is followed by a quantizer consisting of an oscillator and a counter or

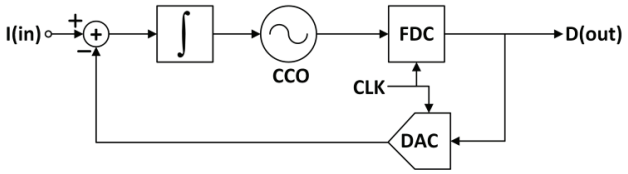

Fig. 1. Circuit topology.

a Frequency-to-Digital converter (FDC). The loop is closed by a Digital-to-Analog converter (DAC).

The topology in this work (Fig. 2) does not use an explicit integrator. However, the integration of the input current is directly performed on the measurement electrode [1], so that a really compact solution is obtained. The resulting voltage is converted back to the current domain by the resistor *R* which is followed by a CCO-based quantizer. A 1-bit current-steering DAC is used to generate the feedback signal.

A. Lossy Integrator Using the Working Electrode as Integration Capacitance

The integrator linearity is crucial for the correct operation of ΔΣ modulators. The charge-transfer resistance R_{EL} (Fig. 2) can lead to a non-linearity issue as reported in [1]. In our application, however, R_{EL} is higher than 1 GΩ and does not represent a limitation, which is also verified by simulation.

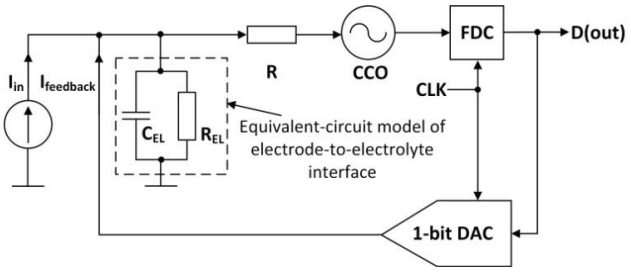

Fig. 2. CCO-based ΔΣ-modulator with signal integration on the working electrode.

B. CCO-Based Quantization Method

The quantization of the oscillator output signal can take place in the time- or in the frequency-domain. In our circuit the latter method is chosen, since it leads to a noise-shaped output signal at very low circuit complexity [11]. This choice requires the clock frequency to satisfy the condition

$$f_{clk} \geq 2 f_{cco,max} \quad . \tag{1}$$

There, f_{clk} is the sampling clock frequency and $f_{cco,max}$ is the maximum oscillation frequency, respectively. The quantization principle is based on the detection of a transition of the oscillator output during the sampling time window. This task is accomplished by a simple digital circuit consisting of two D-flip flops and a XOR-gate, a so-called Frequency-to-Digital Converter (FDC) (Fig. 3). Triggered by the clock edge, the first D-flip flop samples the new oscillator output, while the

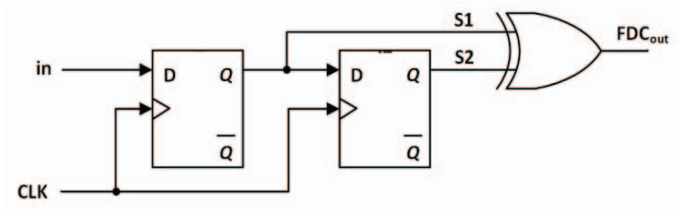

Fig. 3. Frequency-to-Digital converter (FDC).

second D-flip flop holds its previous state sampled during the former clock edge. Both states are delivered to the XOR-gate which outputs a logic "1" if a transition occurs.

C. Current Steering Feedback DAC

For optimum performance in case of a 1st order modulator, the ratio between maximum input current amplitude and feedback current has to be 0.8. In our application, the input current is in the range of ±10 nA, so that a feedback current of ±12 nA is chosen. Although a multibit DAC provides higher modulator resolution, a 1-bit current steering feedback DAC is used here to avoid design reliability problems arising at currents of that order.

III. Circuit Design

The 1st order ΔΣ modulator described above is designed on transistor level and simulated in a 180 nm standard CMOS technology. In this section, design issues are discussed.

A. Current Steering DAC

Since the considered relaxation oscillator (Fig. 7) only sinks current, an offset current has to be fed into the oscillator to guarantee proper operation under all feedback and electrode current conditions. However, instead of combining a DC current with a symmetrical feedback current of ± 12 nA, we chose a simpler solution by shifting both currents by 22 nA so that I_{DC} = 10 nA and $I_{feedback}$ = 0 / +24 nA is used. Consequently, only pMOS current sources are needed.

The current steering DAC is realized using cascode current mirrors (Fig. 4). The cascode transistor M_{casc} shields the drain of the current source transistor M_{source} against capacitive crosstalk from the switching signals applied to M_{41} and M_{switch} and to provide sufficiently high output resistance of the entire current source structure.

When disconnected from the electrode, the current source output is not floating but held at the electrode potential V_{ref} through M_{41}. Otherwise the current source would pull its output node up to the supply voltage, which would lead to long DAC response times and inacceptable voltage variations on the electrode every time when connected to the DAC output.

Two further measures are applied to reduce the DAC's dynamic errors and their impact on the electrode potential. Firstly, the cascode transistor M_{42} buffers the electrode against the parasitic capacitance of switch transistor M_{switch} and thus reduces capacitive crosstalk from the switching signal V_{ctrl}. Secondly, the switch transistors are operated using low swing control signals. The full swing control signal coming from the digital control block is transformed into a low swing control

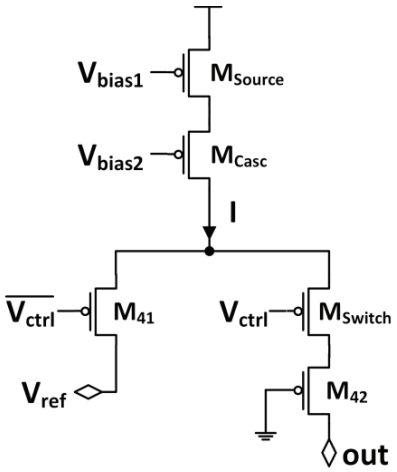

Fig. 4. Unit current source of the current steering DAC.

signals applied to the circuit in Fig. 4. For that purpose, a continuous time bootstrapping circuit is used as depicted in Fig. 5 and similar to the one reported in [12, 13].

There, the source follower M_{55} generates a voltage V_{on} 800 mV below V_{ref}. The driver consisting of M_{51}-M_{54} generates voltage levels between V_{on} and V_{ref} at its output which turn on and off devices M_{41} and M_{swicth} in the current source circuit given in Fig. 4. Devices M_{52} and M_{53} in Fig. 5 attenuate capacitive coupling related effects of fast transitions of V_{ctrl_high} on the circuits output. The effect of the bootstrapping driver circuit is shown in Fig. 6.

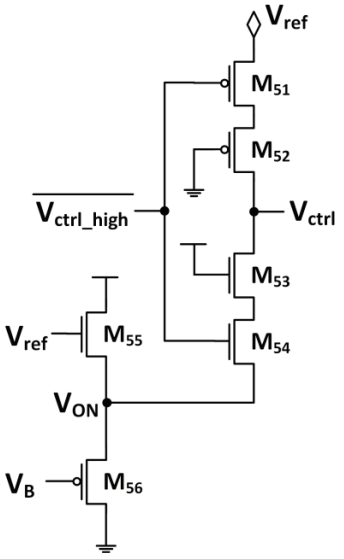

Fig. 5. Continuous-time bootstrapping circuit and control signal driver

B. CCO

As mentioned before, two ΔΣ readout circuits are designed and considered in this work. In the first one, a classical relaxation oscillator is used. In the second, a modified oscillator allows well-controlled sweeping of the electrode voltage.

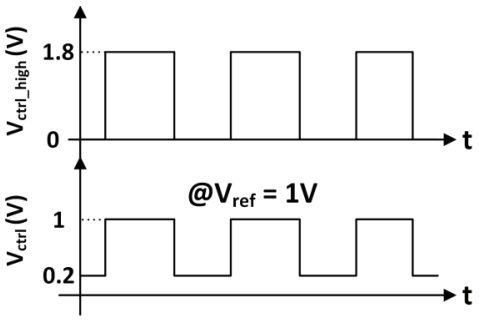

Fig. 6. Control signal transformation.

1) Classical Relaxation Oscillator:

The relaxation oscillator reported in [11] and illustrated in Fig. 7 is suitable for low supply voltage operation. It is designed such that its oscillation frequency does not exceed 2.5 MHz at maximum input current. Its operation principle is based on the integration of the input current until Vint1 (when Vout2 is low) or Vint2 (when Vout1 is low) reaches the respective inverter's threshold voltage. As a consequence the latch state changes. In our case, the integration of the small input current takes place on the parasitic capacitances at the nodes Int1 and Int2. After a number of cycles, the oscillator input settles to the inverter threshold voltage. The use of inverters saves power, since it shortens the latch transition time and reduces the short-circuit current in the oscillator [11].

The electrode voltage ripple depends on the threshold voltage mismatch of the inverters connected to nodes *Int1* and *Int2*. This issue related to random parameter variations can be addressed by sizing up the transistors and using optimized layouts [14]. Here, a trade-off has to be made since gate capacitance increases with transistor size which on the other hand leads to a decrease of the oscillation frequency.

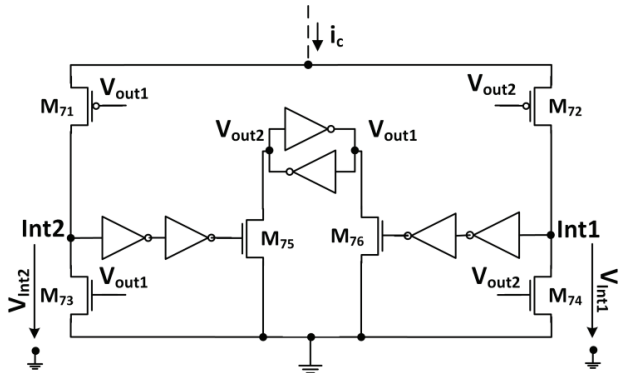

Fig. 7. Classical relaxation oscillator.

2) Modified Relaxation Oscillator:

In the classical oscillator in Fig. 7, two inverter chains change the latch state when the voltage VInt1 or VInt2 reaches the respective threshold voltages. If the inverters are replaced by comparators as shown in Fig. 8, it is possible to change the threshold voltage by changing Vref and the oscillator input node will settle after some oscillation cycles at Vref.

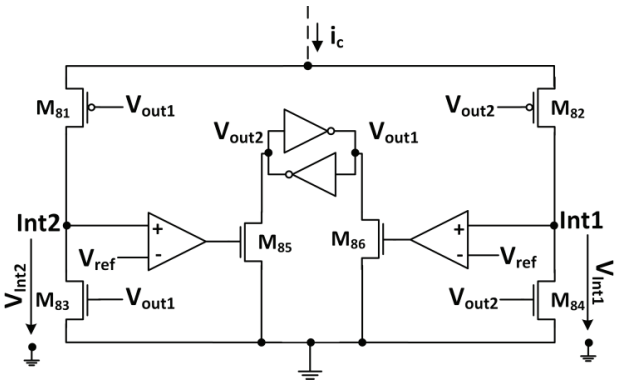

Fig. 8. Relaxtion oscillator with controllable threshold voltage.

Although this approach allows free definition of the threshold voltage, it has major drawbacks. Using two comparators is costly regarding area and power. In fact, the linearity requirements of the oscillator can only be met by using power-hungry high speed comparators. Moreover, the two comparators may have different offset voltages due to device parameter variations. This problem has to be minimized on the cost of a further area increase, otherwise a bigger electrode voltage ripple must be expected. Therefore, a relaxation oscillator with a single high speed comparator (Fig. 10) is used in the second ΔΣ readout circuit.

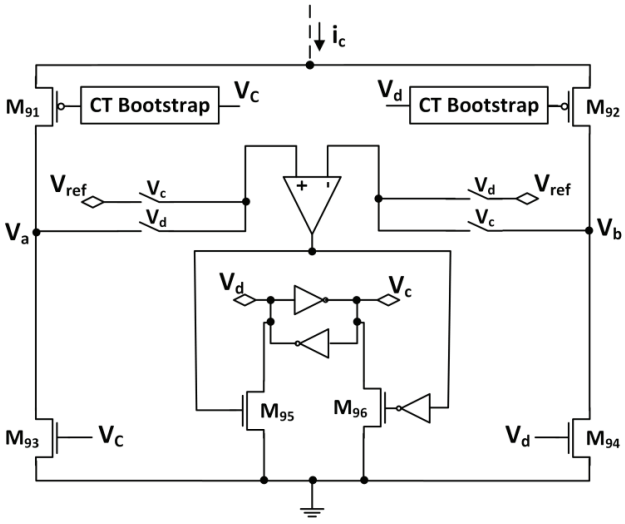

Fig. 9. Relaxation oscillator with single comparator.

In the oscillator in Fig. 7, the switching of M_{71} and M_{72} may affect the electrode voltage. This is prevented using minimum length transistors and connecting their bulk to the supply voltage.

If M_{91} an M_{92} in the oscillator in Fig. 9 are operated directly by the full swing signals V_c and V_d, the solution described above suffers from an increased amount of artifacts: when the electrode voltage is swept to higher voltages, the amplitude of the glitches would increase. M_{91} and M_{92} are turned on by connecting their gates to ground. An increase of the electrode voltage at the oscillator input would translate into a

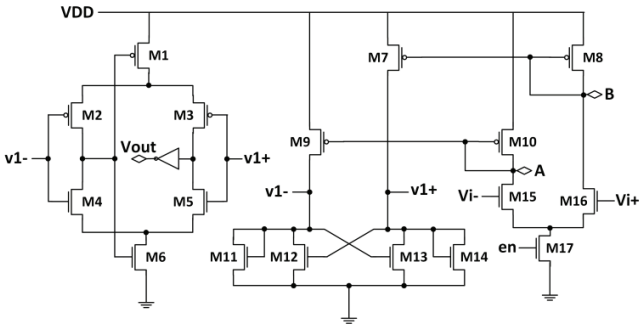

Fig. 10. High speed comparator [14-15]

proportional increase of their on-state overdrive voltage. In other words, the portion of the control signal that couples to the electrode increases. This problem is solved by using continuous-time bootstrapping to drive the gates of M_{91} and M_{92} (Fig. 9). In that way the swing of the switching signals is kept low and uniform over the whole V_{ref} voltage range.

C. Electrode Voltage Offset Cancellation

As mentioned before, the oscillator input settles after some cycles at the comparator threshold voltage. The same applies to the electrode. For the cyclovoltammetric procedure, the electrode voltage has to be carefully controlled and its deviation from V_{ref} has to be kept within certain limits of the order ±10 mV.

This issue is solved by calibration. The depicted calibration circuit in Fig. 11 injects current into the outputs of the comparator preamplifier (nodes A and B) to shift the comparator switching point and to compensate for possible input-referred offset voltages.

The calibration process is illustrated in Fig. 12. In a first step, the calibration circuit injects maximum current into node A and decreases it gradually. In that way, it generates a controlled input referred offset and decreases it from maximum to minimum. In a second step, the current is injected into node B, which results in an offset of opposite sign. This time, the current is swept from minimum to maximum, as well as the offset. When the generated offset value cancels the circuit offset, the comparator output changes. The configuration of the switches *S1-S8* at transition time is memorized and kept during the readout operation. The amount of current delivered by each calibration unit current source causes an offset change of 3 mV per step. This value corresponds to the maximum remaining offset after calibration.

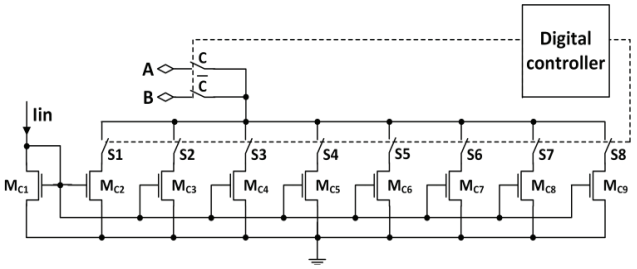

Fig. 11. Calibration circuit.

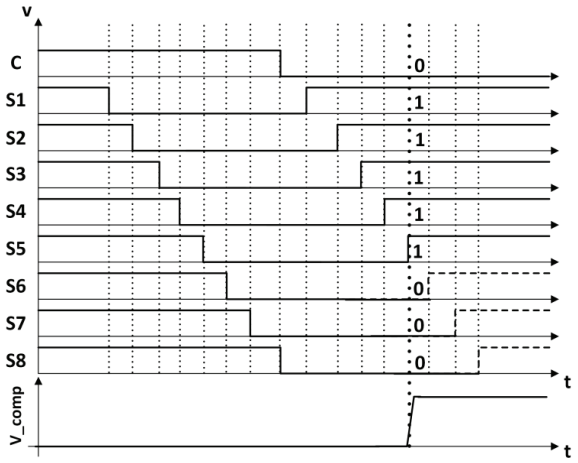

Fig. 12. Calibration process and memorized switch configuration.

IV. Simulation Results

As input signal, a sinusoidal current with 10 nA amplitude and 1 kHz frequency is chosen, the clock frequency equals 6 MHz. The band of interest is 10 kHz, which is typical for our application.

The modulator based on the classical relaxation oscillator achieves an SNDR of 67 dB. Its output spectrum depicted in Fig. 13 reveals a noise shaping of 30 dB/decade. The modulator based on the modified relaxation oscillator achieves under the same conditions an SNDR of 62 dB and a similar noise shaping (Fig. 14).

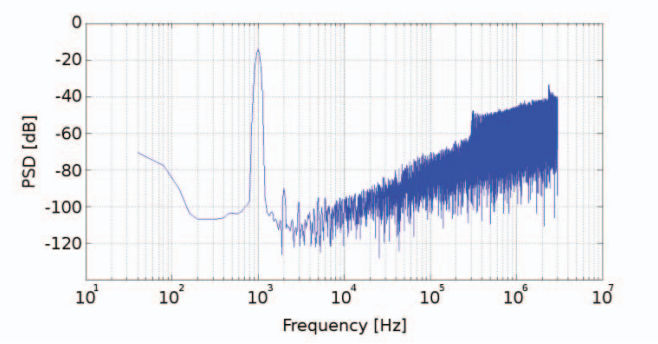

Fig. 13. FFT output spectrum of the ΔΣ modulator with classical CCO.

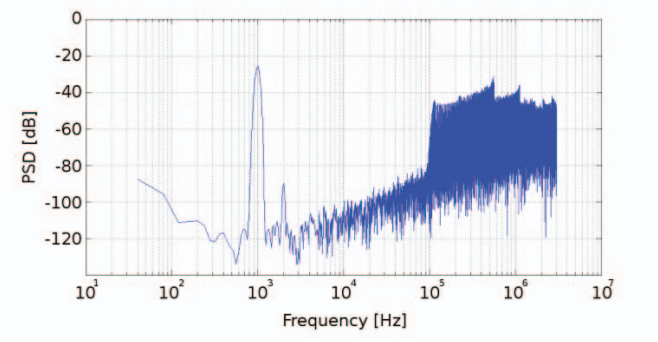

Fig. 14. FFT output spectrum of the ΔΣ modulator with modified CCO.

This can be explained by considering two issues: on the one hand, the CCO-based quantizer achieves 1st order noise shaping and enhances the global noise shaping. On the other hand, the integration on the electrode capacitance does not provide gain at low frequencies as a conventional operational amplifier-based integrator does. This leads to noise shaping deterioration. Consequently, instead of a 2nd order noise shaping of 40 dB/decade, we obtain 30 dB/decade.

As expected, the electrode voltage obtained in the first case settles at the inverter threshold voltage (Fig. 14). It shows limited switching artifacts thanks to oscillator switching rapidness and to the resistor *R* in Fig. 2.

The second readout circuit allows sweeping of the electrode voltage up and down over a range of 500 mV as required for the voltammetric readout procedure (Fig. 16). This is achieved by sweeping the voltage V_{ref} (cf. Fig. 9). Furthermore, the electrode voltage ripple is about 6 mV and its offset is kept within acceptable limits.

Resolution, power consumption, and estimated area of both circuits are summarized in Table 1.

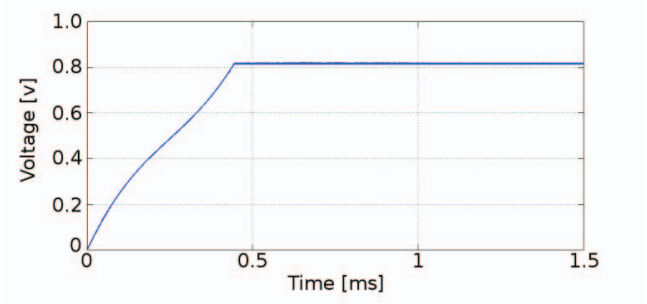

Fig. 15. Electrode voltage during readout with classical CCO.

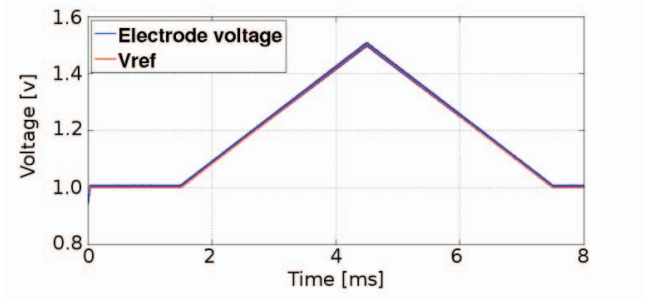

Fig. 16. Electrode voltage during readout using the modified CCO.

TABLE I.
Circuit Characteristics

	Modulator with classical oscillator (Fig. 7)	Modulator with modified oscillator (Fig. 9)
SNDR	67 dB	62.0 dB
Power consumption	80 µW	52.2 µW
Estimated area (180 nm std. process)	1500 µm²	5000 µm²

V. CONCLUSION

A 1st order current-mode ΔΣ modulator architecture suitable for electrochemical detection is presented. The proposed topology is highly efficient regarding area and power thanks to signal integration on the electrode-to-electrolyte capacitance and CCO-based quantization. Two transistor-level implementations are presented and design aspects related to the requirements of electrochemical detection are discussed. In the second implementation, a modified relaxation oscillator is used in the ΔΣ-loop. Simulation results are considered to evaluate the suitability and performance of the two approaches. Both implementations achieve 30 dB/decade noise shaping and reach an SNDR of 67.3 and 62.0 dB, respectively, at a signal bandwidth of 10 kHz.

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